Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-90. (canceled)

91. (new) A method comprising:

setting a first processor in a processing system to operate in an isolated execution mode, wherein the first processor supports (a) the isolated execution mode in a ring 0 operating mode, (b) a normal execution mode in the ring 0 operating mode, and (c) one or more higher ring operating modes;

configuring the processing system to establish an isolated memory area in a memory of the processing system;

detecting, at the first processor, a snoop transaction from a second processor; and

disallowing the snoop transaction if (a) the snoop transaction requests access to an address that is cached by the first processor, (b) said address resides in the isolated memory area, and (c) the second processor is not set to operate in the isolated execution mode.

92. (new) A method according to claim 91, further comprising:

detecting, at the first processor, a transaction that requests access to the memory of the processing system; and

disallowing the transaction if (a) the transaction involves the isolated memory area and (b) the first processor is not set to operate in the isolated execution mode.

93 (new) A method according to claim 92 further comprising:

in response to detecting the transaction that requests access to the memory, determining, based at least in part on a physical address from a translation lookaside buffer (TLB) of the processor, whether the transaction involves the isolated memory area.

94. (new) A method according to claim 91, wherein the operation of detecting a snoop transaction from a second processor comprises:

receiving the snoop transaction from a front side bus (FSB) responsive to the first processor.

95. (new) A method according to claim 91, wherein the operation of detecting a snoop transaction from a second processor comprises:

receiving the snoop transaction from a front side bus (FSB), wherein the snoop transaction specifies a physical address to be accessed.

96. (new) A method according to claim 91, further comprising:

disallowing snoop transactions involving addresses that reside in the isolated memory area if the first and second processors are not both set to operate in the isolated execution mode.

97. (new) A method according to claim 91, wherein the operation of disallowing the snoop transaction is performed by an access checking circuit of the first processor.

98. (new) A method according to claim 91, further comprising:

determining, based at least in part on an isolated execution mode setting in a processor control register of the first processor, whether the first processor is set to operate in the isolated execution mode.

99. (new) An apparatus for use in a processing system having memory, the apparatus comprising:

a first processor for a processing system, wherein the first processor supports (a) an isolated execution mode in a ring 0 operating mode, (b) a normal execution mode in the ring 0 operating mode, and (c) one or more higher ring operating modes, the processor operable to detect a snoop transaction from a second processor; and

an access checking circuit in the first processor, the access checking circuit operable to disallow the snoop transaction if (a) the snoop transaction requests access to an address that is cached by the first processor, (b) said address resides in an isolated memory area in a memory of the processing system, and (c) the second processor is not set to operate in the isolated execution mode.

100. (new) An apparatus according to claim 99, further comprising:

the first processor operable to detect a memory transaction that requests access to the memory of the processing system; and

the access checking circuit operable to disallow the memory transaction if (a) the memory transaction involves the isolated memory area and (b) the first processor is not set to operate in the isolated execution mode.

101. (new) An apparatus according to claim 100, wherein the memory transaction comprises a transaction generated during execution of an instruction in the first processor.

102. (new) An apparatus according to claim 101, further comprising:

a translation lookaside buffer (TLB) in the first processor; and

the access checking circuit operable to determine, based at least in part on a physical address from the TLB, whether the memory transaction involves the isolated memory area.

103. (new) An apparatus according to claim 100, further comprising:

the first processor operable to assert a signal to grant access for the memory transaction if the first processor is set to operate in the isolated execution mode.

104. (new) An apparatus according to claim 99, further comprising:

the access checking circuit operable to determine whether to allow the snoop transaction based at least in part on a cache access signal from the first processor and an isolated access signal from the second processor.

105. (new) An apparatus according to claim 99, further comprising:

the access checking circuit operable to disallow snoop transactions from the second processor involving the isolated memory area if the first and second processors are not both set to operate in the isolated execution mode.

106. (new) A processing system comprising:

first and second processors that can each be set to operate in a normal execution mode in a ring 0 operating mode and, alternatively, to operate in an isolated execution mode in the ring 0 operating mode, wherein the first processor also supports one or more higher ring operating modes, the first processor operable to detect a snoop transaction from the second processor;

memory to include an isolated memory area, the memory responsive to the first processor; and

an access checking circuit in the first processor, the access checking circuit operable to disallow the snoop transaction if (a) the snoop transaction requests access to an address that is cached by the first processor, (b) said address resides in the isolated memory area, and (c) the second processor is not set to operate in the isolated execution mode.

107. (new) A processing system according to claim 106, further comprising:

the first processor operable to detect a memory transaction that requests access to the memory of the processing system; and

the access checking circuit operable to disallow the memory transaction if (a) the memory transaction involves the isolated memory area and (b) the first processor is not set to operate in the isolated execution mode.

108. (new) A processing system according to claim 107, wherein:

the memory transaction comprises a transaction generated during execution of an instruction in the first processor.

109. (new) A processing system according to claim 107, further comprising:

a translation lookaside buffer (TLB) in the first processor; and

the access checking circuit operable to determine, based at least in part on a physical address from the TLB, whether the memory transaction involves the isolated memory area.

110. (new) A processing system according to claim 107, further comprising:

the first processor operable to assert a signal to grant access for the memory transaction if the first processor is set to operate in the isolated execution mode.

111. (new) A processing system according to claim 106, further comprising:

the access checking circuit operable to determine whether to allow the snoop transaction based at least in part on a cache access signal from the first processor and an isolated access signal from the second processor.

112. (new) A processing system according to claim 106, further comprising:

the access checking circuit operable to disallow snoop transactions from the second processor involving the isolated memory area if the first and second processors are not both set to operate in the isolated execution mode.